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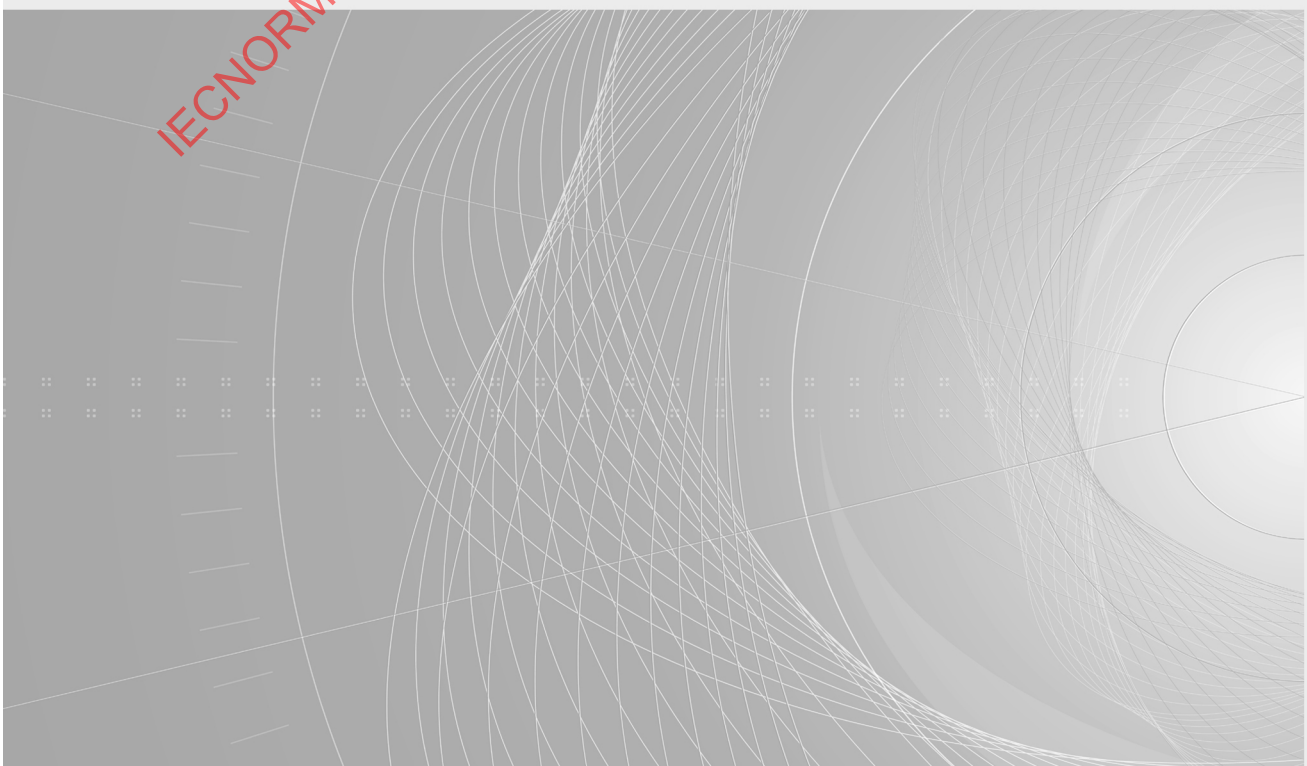
Edition 1.0 2016-08

TECHNICAL REPORT

Electrical interface specification for phase-cut dimmer in phase-cut dimmed lighting systems



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INTERNATIONAL
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CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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ELECTRICAL INTERFACE SPECIFICATION FOR PHASE-CUT DIMMER IN PHASE-CUT DIMMED LIGHTING SYSTEMS

FOREWORD

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IEC TR 63036, which is a technical report, has been prepared by subcommittee 23B: Plugs, socket-outlets and switches, of IEC technical committee 23: Electrical accessories.

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
23B/1201/DTR	23B/1214/RVC

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

INTRODUCTION

This document describes the technical requirements for phase-cut dimmers to work with controlgear and self ballasted lamps. For a complete picture of the technical requirements the reader should also refer to IEC TR 63037 that contains technical requirements and testing methods for controlgear and self ballasted lamps.

ELECTRICAL INTERFACE SPECIFICATION FOR PHASE-CUT DIMMER IN PHASE-CUT DIMMED LIGHTING SYSTEMS

1 Scope

This technical report specifies the electrical interface and test procedures for the control by mains voltage phase-cut dimming of the brightness of mains operated electronic lighting equipment intended to be controlled by mains voltage phase-cut dimmers, such as LED integrated lamps, and light sources with external control gear.

Electronic switches that use a comparable circuitry to a phase-cut dimmer but do not contain means for the adjustability of the phase-cut angle should fulfill the same requirements as a phase-cut dimmer.

Safety requirements are not covered by this document, but by respective product standards.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60038, *IEC standard voltages*

IEC 60050-845, *International Electrotechnical Vocabulary (IEV) – Part 845: Lighting* (available at www.electropedia.org)

IEC 60364 (all parts), *Low-voltage electrical installations*

IEC 62504, *General lighting – Light emitting diode (LED) products and related equipment – Terms and definitions*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 62504 and IEC 60050-845 as well as the following apply.

3.1
lighting system
combination of a phase-cut dimmer and one or more controlgear and light sources

3.2
off state
state of a lighting system when no light is emitted

3.3
on state
state of a lighting system when light is emitted

3.4
electrical interface
electrical parameters for supplying power and making the exchange of information between the phase-cut dimmer and controlgear possible

3.5

phase-cut dimmer
electronic switch that is connected in series with a load and changes the supply voltage waveform applied to the load from the pure mains voltage waveform to a leading edge (forward phase) or a trailing edge (reverse phase) AC voltage waveform or is capable of switching between both waveforms

Note 1 to entry: The output voltage waveform of a phase-cut dimmer is applied to one or more loads.

Note 2 to entry: The conduction angle of the voltage waveform is adjustable.

Note 3 to entry: Within this document, where the term “dimmer” is used the term “phase-cut dimmer” is meant.

3.6
two-wire phase-cut dimmer
phase-cut dimmer that is connected in series with the load and has no connection to neutral

3.7
three-wire phase-cut dimmer
phase-cut dimmer that is connected in series with the load and has in addition a connection to neutral

3.8
controlgear
device between the phase-cut dimmer and one or more lamps which may serve to transform the AC mains power, limit the current of the lamp(s) to the required value, provide starting voltage and preheating current, prevent cold starting, correct power factor or reduce radio interference

Note 1 to entry: Lamps may have integrated controlgear such as an integrated LED lamp. Any references to controlgear will include any such integrated lamps.

3.9
load side
wire from the output of the phase-cut dimmer to the supply input of one or more controlgear

3.10
conducting period
time period during which the phase-cut dimmer supplies power to a controlgear

3.11
non-conducting period
time period during which the phase-cut dimmer does not supply power to a controlgear

3.12
half wave
positive or negative 180° of an AC sine wave starting and ending at the zero crossing point

3.13
phase angle
position within a half wave expressed in degree, being in the range of 0° to 180°, in reference to the beginning of the half wave

4 General description

A phase-cut dimmer either cuts the mains voltage immediately after the zero crossing of the mains (leading edge) or towards the next projected zero crossing of the mains (trailing edge). The functionality of both methods may be implemented in one device (universal dimmers).

This document describes requirements for phase-cut dimmers during the on state of a lighting system. Specifications are provided dependent on the dimming method for the conducting period and the non-conducting period of the phase-cut dimmer and the transitions between conducting and non-conducting period.

In addition, this document describes requirements for phase-cut dimmers during the off state of a lighting system. Specifications are provided independently from the dimming method.

5 General requirements

5.1 Voltage rating

This document applies to one or more of the following mains voltages:

100 V, 120 V, 200 V, 230 V, 277 V, according to IEC 60038.

5.2 Frequency rating

This document applies to one or more of the following mains frequencies:

50 Hz or 60 Hz, according to IEC 60038.

5.3 Marking of phase-cut dimmer

The following information should be provided by the manufacturer on the product or in the accompanying instruction sheets.

Phase-cut dimmers requiring more than one controlgear to function properly should be marked with the required minimum number of connected controlgear.

Phase-cut dimmers requiring a minimum load should be marked with the required minimum load.

Phase-cut dimmers should be marked with the following indication:

DIM

6 Description of the lighting system and its components

6.1 Wiring method

The wiring of the devices is in accordance with the installation rules given in the IEC 60364 series and also with the national wiring rules applicable in the country where the devices are installed.

6.2 Wiring diagram

The wiring of the lighting system uses the traditional method of connecting the phase-cut dimmer to the mains and to the controlgear. Figure 1 is an example of a lighting system with one phase-cut dimmer and one or two controlgear(s).

Regarding the connections of the phase-cut dimmer shown in Figure 1, the drawn lines represent a two-wire installation and the dashed line represents the direct connection of the phase-cut dimmer to the mains which is used in three-wire installations.

The direct connection of the phase-cut dimmer to neutral (dashed line in Figure 1) will have consequences on the power supply requirements and synchronization to the phase-cut dimmer.

This document defines requirements that enable compatibility between phase-cut dimmers and controlgear in two-wire installations. However, all predications are also valid for three-wire phase-cut dimmers to ensure proper operation of controlgear.

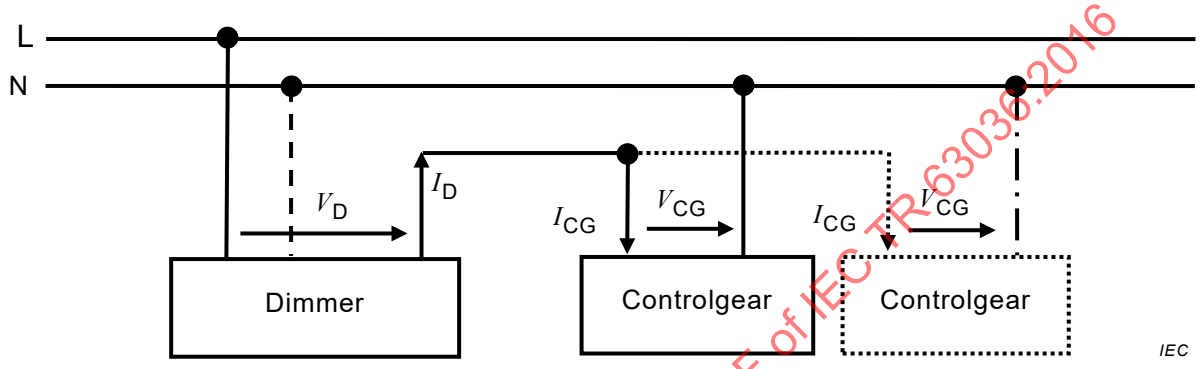

Figure 1 – Example of wiring diagram

7 Electrical specification

7.1 Overview

To describe the electrical characteristics of the electrical interface, the following abbreviations are used:

α_x Angle where the test voltage starts rising with the given slew rate SR as shown in Figure A.1

β_x Angle where the test voltage starts falling with the given slew rate SR as shown in Figure A.2

C_f Filter capacitor to reduce high frequency disturbances

EC_CG Equivalent circuit that represents a controlgear for phase-cut dimmer testing purposes

EC_D Equivalent circuit that represents a phase-cut dimmer for controlgear testing purposes

I_{CG} Current through the input terminals of the controlgear (see Figure 1)

I_{CG_pk} Repetitive peak current of the controlgear in leading edge mode

I_{CG_SL} Current-carrying capability of the controlgear with $V_{CG} \leq V_{SW}$ in leading edge mode

I_{CG_STH} Current -carrying capability of the controlgear with $V_{CG} \leq V_{SW}$ in trailing edge mode

I_{CG_STL} Current-carrying capability of the controlgear with $V_{CG} > V_{SW}$ in trailing edge mode

I_D Current through the load side terminal of the phase-cut dimmer (see Figure 1)

I_{D_nc} Maximum current through the phase-cut dimmer during the non-conducting period, limited by the phase-cut dimmer

I_{PO} Minimum current carrying capability of the controlgear during the electronic off state

I_{trans} Current sourced by the phase-cut dimmer during the transition from the conducting to the non-conducting state in trailing edge mode

n Required minimum number of controlgear connected with one phase-cut dimmer (named in phase-cut dimmer installation sheet)

P_{CG} Rated input power of the controlgear (as marked)

P_{max} Maximum permissible nominal load of phase-cut dimmer (according to the installation sheet)

P_{min} Minimum nominal load required by phase-cut dimmer (according to the installation sheet)

R_R Resistance value of ohmic load R in relation to the relevant mains voltage according to Tables 7 to 11, representing the maximum permissible load of phase-cut dimmer P_{max}

SR Absolute value of the slew rate of the decrease of the voltage across the input terminals of a controlgear in trailing edge dimming mode when the phase-cut dimmer switches off at time t_{s1} (see Figure 3)

SR_L Absolute value of the slew rate of the increase of the voltage across the input terminals of a controlgear in leading edge dimming mode when the phase-cut dimmer under test switches on (according to Clause 8)

SR_T Absolute value of the slew rate of the decrease of the voltage across the input terminals of a controlgear in trailing edge dimming mode when the phase-cut dimmer under test switches off (according to Clause 8)

t_{HW} Time related to previous zero crossing of the mains to the subsequent zero crossing of the mains (duration of a half wave)

t_s Time related to previous zero crossing of the mains when leading edge phase-cut dimmer reduces its impedance towards zero by activating its power switch

t_{s1} Time related to previous zero crossing of the mains when trailing edge phase-cut dimmer increases its impedance towards infinite by deactivating its power switch

t_{s2} Time related to previous zero crossing of the mains when the voltage V_{CG} falls below V_{SW} in trailing edge method

t_{s3} Time related to previous zero crossing of the mains when the transition from the conducting period to the non-conducting period is finished

t_{SW} Time related to previous zero crossing of the mains when voltage V_{CG} crosses V_{SW}

t_t Transition time for trailing edge mode, equals $t_{s2} - t_{s1}$

V_{CG} Voltage across the input terminals of the controlgear (see Figure 1)

V_D Voltage between the line side (L) and load side terminal of the phase-cut dimmer (see Figure 1)

V_M Mains voltage (rated nominal value)

V_{ME} Phase-cut voltage for testing purposes, sinusoidal part of the waveform (α_1 to t_{HW}, 0 to β) equivalent to mains voltage

V_{PO} Lower limit for voltage across the input terminals of the controlgear to provide a current carrying capability I_{PO} during the electronic off state

V_{SW} Voltage across the input terminals of the controlgear at the time that leads to disabling ($V_M(t) > V_{SW}$) or enabling ($V_M(t) < V_{SW}$) a current path having a current carrying capability of I_{CG_SL} or I_{CG_STH}

V_{test} Value of test voltage (according to 8.3 of IEC TR 63037:–)

$xx(t)$ Instantaneous values of current or voltage xx

Z_{CG} Impedance across the input terminals of the controlgear

Z_D Impedance between the line side (L) and the load side terminals of the phase-cut dimmer

Z_{D_max} Maximum impedance between the line side (L) and load side terminal of the phase-cut dimmer, defined by the technical properties of the phase-cut dimmer

Z_{D_min} Minimum impedance between the line side (L) and the load side terminal of the phase-cut dimmer, defined by the power properties of the phase-cut dimmer

7.2 General

All information given in this document is related to a half wave of the mains. Due to the polarity change between subsequent half waves, all values have to be regarded as absolute values.

The lighting system is either in on state or in off state. In on state, light sources controlled by controlgear being part of the lighting system emit light. In off state, light sources controlled by controlgear being part of the lighting system do not emit light.

The off state may be realized as mechanical off state by opening the current loop of the lighting system with mechanical means, for example a switch. For this case, no requirements need to be fixed.

Alternatively, the off state may be realized as electronic off state. In this case, the phase-cut dimmer increases its impedance (i.e. stops producing phase-cut) while continuing its operation, for example to keep its control interface activated. In this case, the connected controlgear is not energized sufficiently to operate a light source, but provides a current path that allows the phase-cut dimmer to draw current continuously from the mains.

NOTE Applications that provide a connection to neutral allow the use of a three-wire device, enabling the usage of lamps that do not provide a current carrying capability according to 7.3 and 7.4.

During the on state and the electronic off state, it should be ensured that the phase-cut dimmer is supplied sufficiently with power and that the synchronization of phase-cut dimmer and controlgear with the mains is ensured.

7.3 Electrical characteristics during the on state of a lighting system

7.3.1 General

For the on state of a lighting system, specifications are dependent on the dimming method, leading edge or trailing edge.

Each half wave is divided into two periods, the conducting period and the non-conducting period of the phase-cut dimmer.

During the conducting period of the phase-cut dimmer, the mains voltage is applied to the controlgear. During the non-conducting period, the voltage between terminals of the phase-cut dimmer is almost equal to the mains voltage ($V_D \approx V_M$).

7.3.2 Electrical characteristics for leading edge dimming method

7.3.2.1 General

Starting from the mains zero crossing, the phase-cut dimmer remains in a non-conducting state until its timing element activates the power switch at t_s. Afterwards, the phase-cut dimmer supplies power to the load for the entire remaining part of the mains half wave (see Figure 2).

To achieve synchronization with the mains and to control the phase-cut angle correctly, leading edge phase-cut dimmers need to draw a current also during the non-conducting state.

Thus, the controlgear is able to conduct a current I_{CG_SL}, which allows synchronization of the phase-cut dimmer with the mains and ensures the supply of power to the phase-cut dimmer even in a two-wire installation.

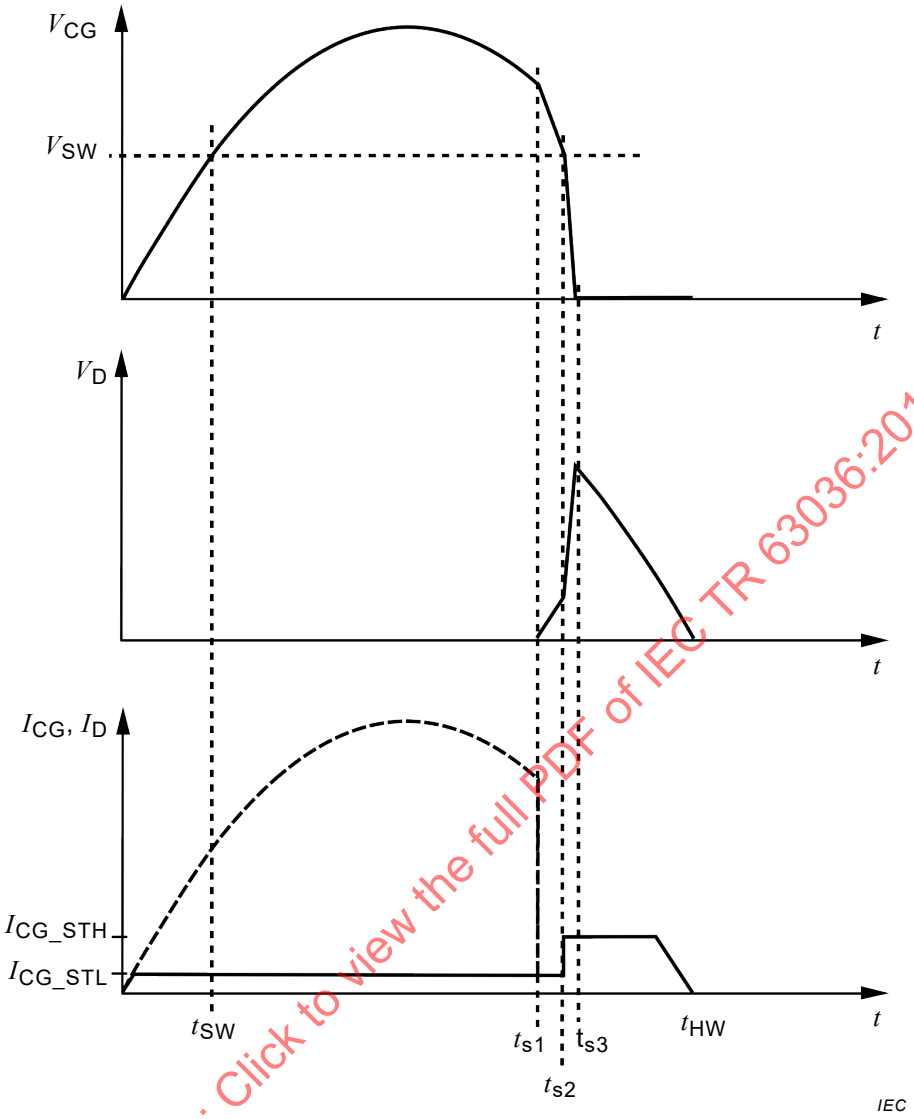

Figure 2 – Timing leading edge dimming method

7.3.2.2 Electrical characteristics during the non-conducting period

During the non-conducting period, the phase-cut dimmer should comply with the electrical characteristics listed in Tables 1 to 5.

The non-conducting period starts at the zero crossing of the mains and ends at time t_s when the timing element of the phase-cut dimmer activates the power switch.

During this period, the controlgear provides a current path with a minimum current-carrying capability of I_{CG_SL}.

The controlgear may deactivate its current-carrying capability during the non-conducting period after it has not detected an input voltage waveform showing an unsteady waveform (leading edge characteristic) for 100 ms.

NOTE This is for reducing power losses in case a controlgear is used without a phase-cut dimmer.

During this period, the phase-cut dimmer should limit the current I_D to n x I_{D_nc} as listed in the Tables 1 to 5, whereby I_{D_nc} is related to P_{min} of the phase-cut dimmer.

EXAMPLE For Table 4: $I_D(t) \leq I_{D\_nc} = n$ x 5,4 mA/W x P_{min} With n = 2(number of lamps), P_{min} of the dimmer equals 3 W, then $I_D(t)$ is lower than 32,4mA.

Table 1 – Nominal mains voltage 100 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Current limits
0 to t_s	P_{min} < 12 W: $I_D(t) \leq I_{D\_nc}$ = n x 12,4 mA/W x P_{min} $P_{min} \geq$ 12 W: $I_D(t) \leq I_{D\_nc} = n$ x 149 mA

Table 2 – Nominal mains voltage 120 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Current limits
0 to t_s	P_{min} < 12 W: $I_D(t) \leq I_{D\_nc}$ = n x 10,4 mA/W x P_{min} $P_{min} \geq$ 12 W: $I_D(t) \leq I_{D\_nc} = n$ x 124,2 mA

Table 3 – Nominal mains voltage 200 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Current limits
0 to t_s	P_{min} < 12 W: $I_D(t) \leq I_{D\_nc}$ = n x 6,2 mA/W x P_{min} $P_{min} \geq$ 12 W: $I_D(t) \leq I_{D\_nc} = n$ x 74,5 mA

Table 4 – Nominal mains voltage 230 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Current limits
0 to t_s	P_{min} < 12 W: $I_D(t) \leq I_{D\_nc}$ = n x 5,4 mA/W x P_{min} $P_{min} \geq$ 12 W: $I_D(t) \leq I_{D\_nc} = n$ x 65 mA

Table 5 – Nominal mains voltage 277 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Current limits
0 to t_s	P_{min} < 12 W: $I_D(t) \leq I_{D\_nc}$ = n x 4,5 mA/W x P_{min} $P_{min} \geq$ 12 W: $I_D(t) \leq I_{D\_nc} = n$ x 54 mA

7.3.2.3 Electrical characteristics during transition from the non-conducting to the conducting period

The transition from the non-conducting to the conducting state of the phase-cut dimmers starts at time t_s.

Starting from time t_s, the impedance Z_D of the phase-cut dimmer decreases until its minimum Z_{D_min} is reached. The voltage V_{CG} applied to the controlgear increases towards the instantaneous value $V_M(t)$ of the mains minus the voltage drop across the phase-cut dimmer.

The absolute value of the slew rate of the voltage change of V_D during the transition period should not exceed the values as listed in Table 6 when the phase-cut dimmer is connected to the marked maximum resistive load.

The slew rate should be calculated based on the measurement of the voltage slope of V_D by measuring the time (dt) between V_D = 0,8 x $V_D(t_s)$ and V_D = 0,1 x $V_D(t_s)$ and by calculating the differential voltage dV_D = 0,8 x $V_D(t_s)$ – 0,1 x $V_D(t_s)$.

When the voltage V_{CG} exceeds V_{SW}, the controlgear may deactivate its bypass circuitry (see Figure 2), thus possibly no current can flow through the controlgear.

NOTE Values for slew rate represent a compromise between EMC, repetitive peak current in the controlgear and switching losses in the phase-cut dimmer power semiconductors.

Table 6 – Slew rate for voltage decrease across the phase-cut dimmer

V_M [V]	100	120	200	230	277
$\lvert dV_D/dt \rvert$ [V/µs]	≤ 6,5	≤ 300	≤ 6,5	≤ 6,5	≤ 300

7.3.2.4 Electrical characteristics during the conducting period

During the conducting period, the phase-cut dimmer should comply with the electrical characteristics listed in Tables 7 to 11.

During this period, full power should be applied continuously to the controlgear from the phase-cut dimmer to allow power to be supplied to the controlgear.

During this period, independently from the current $I_D = I_{CG}$, the impedance Z_D of the phase-cut dimmer should remain constantly at its minimum value Z_{D_min}.

The impedance Z_D of the phase-cut dimmer is Z_{D_min} when the voltage $V_D(t)$ across the phase-cut dimmer is less than 0,1 x $V_M(t)$ during the entire conduction period.

NOTE Multiple switching cycles of the power switch during the conducting period result in non-constant Z_D of the phase-cut dimmer. This is not desired.

Due to the low impedance of the phase-cut dimmer during the conducting period, the input voltage of the controlgear is almost equal to the mains voltage.

At time t_{sw}, the input voltage V_{CG} of the controlgear falls below V_{SW}.

From time t_{sw} to the end of the period, the controlgear provides a current path with a minimum current-carrying capability of I_{CG_SL}.

Table 7 – Nominal mains voltage 100 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Impedance
t_s to t_{sw}	$Z_D = Z_{D\_min}$ $V_D(t) < \max(0{,}1 \times V_M(t), 10\ V)$ NOTE At t_s, Z_D starts to decrease
t_{sw} to t_{HW}	$Z_D = Z_{D\_min}$ $V_D(t) < \max(0{,}1 \times V_M(t), 10\ V)$

Table 8 – Nominal mains voltage 120 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Impedance
t_s to t_{sw}	$Z_D = Z_{D\_min}$ $V_D(t) < \max(0{,}1 \times V_M(t), 10\ V)$ NOTE At t_s, Z_D starts to decrease
t_{sw} to t_{HW}	$Z_D = Z_{D\_min}$ $V_D(t) < \max(0{,}1 \times V_M(t), 10\ V)$

Table 9 – Nominal mains voltage 200 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Impedance
t_s to t_{sw}	$Z_D = Z_{D\_min}$ $V_D(t) < \max(0{,}1 \times V_M(t), 10\ V)$ NOTE At t_s, Z_D starts to decrease
t_{sw} to t_{HW}	$Z_D = Z_{D\_min}$ $V_D(t) < \max(0{,}1 \times V_M(t), 10\ V)$

Table 10 – Nominal mains voltage 230 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Impedance
t_s to t_{sw}	$Z_D = Z_{D\_min}$ $V_D(t) < \max(0{,}1 \times V_M(t), 10\ V)$ NOTE At t_s, Z_D starts to decrease
t_s to t_{sw}	$Z_D = Z_{D\_min}$ $V_D(t) < \max(0{,}1 \times V_M(t), 10\ V)$

Table 11 – Nominal mains voltage 277 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Impedance
t_s to t_{sw}	$Z_D = Z_{D\_min}$ $V_D(t) < \max(0{,}1 \times V_M(t), 10\ V)$ NOTE At t_s, Z_D starts to decrease
t_s to t_{sw}	$Z_D = Z_{D\_min}$ $V_D(t) < \max(0{,}1 \times V_M(t), 10\ V)$

7.3.3 Electrical characteristics for trailing edge dimming method

7.3.3.1 General

Starting from the mains zero crossing, the phase-cut dimmer operates in conducting state until its timing element deactivates the power switch at time t_{s1}. Afterwards, the phase-cut dimmer is not significantly supplying power to the load for the entire remaining part of the mains half wave (see Figure 3).

To achieve synchronization with the mains and to control the phase-cut angle correctly, trailing edge phase-cut dimmers need to draw a current also during the non-conducting state.

Thus, the controlgear is able to conduct a current I_{CG_STH}, which allows synchronization of the phase-cut dimmer with the mains and ensures the supply of power to the phase-cut dimmer even in a two-wire installation.

Since the negative voltage slope that is triggered by the switch-off of the power switch of the phase-cut dimmer is not only determined by the current I_{CG_STL} that is conducted by the controlgear, but also by the effective capacitance of the wiring and the capacitance being effective in parallel to the phase-cut dimmer, the sum of these capacitances has to be considered.

This document and all listed values are based on systems having a maximum capacitance of the wiring of 10 nF being effective in parallel to the controlgear.

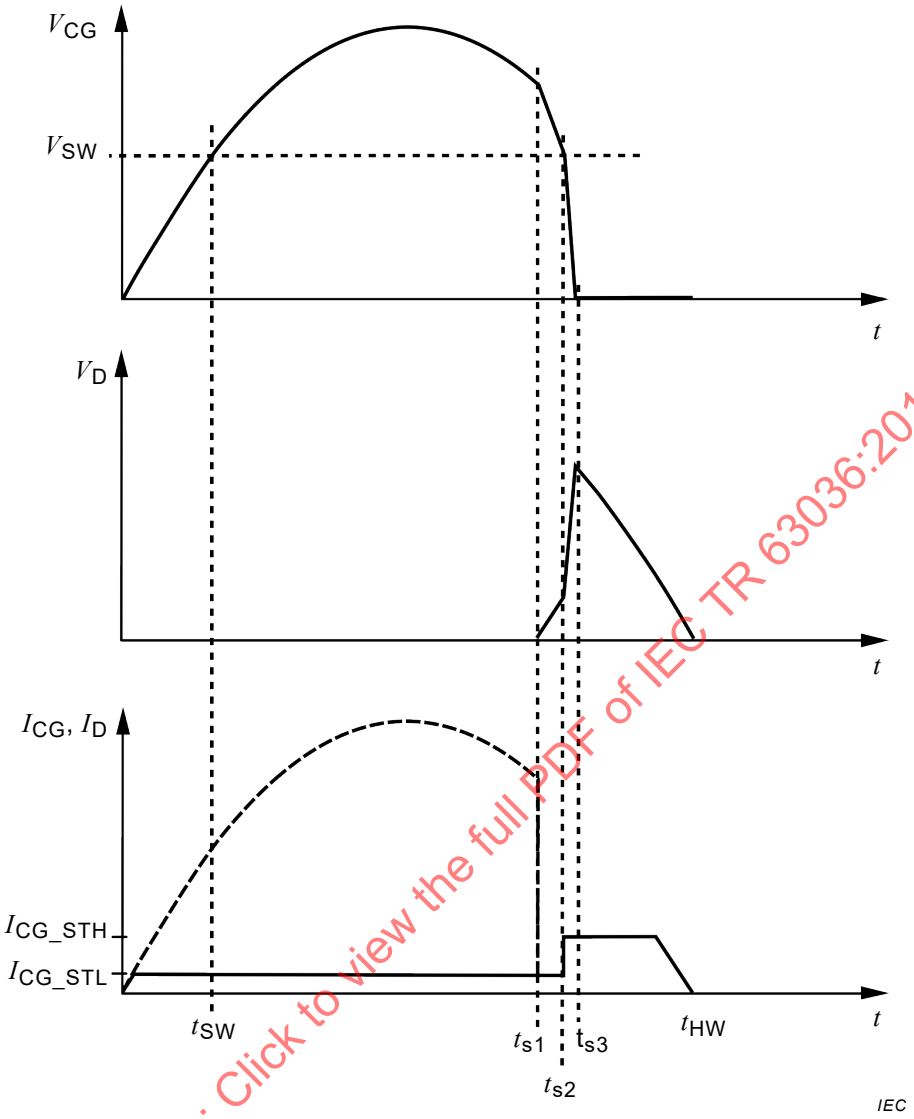

Figure 3 – Timing trailing edge dimming method

7.3.3.2 Electrical characteristics during the conducting period

The conducting period starts at the zero crossing of the mains and ends at time t_{s1} when the timing element of the phase-cut dimmer deactivates the power switch and the impedance of the phase-cut dimmer Z_D increases towards Z_{D_max}.

During the conducting period, the phase-cut dimmer should comply with the electrical characteristics listed in Table 12.

During this period, the phase-cut dimmer should continuously apply full power to the controlgear. Therefore, the impedance Z_D of the phase-cut dimmer should remain continuously at its minimum value Z_{D_min}, independently from the current $I_D = I_{CG}$.

The impedance Z_D of the phase-cut dimmer is Z_{D_min} when the voltage $V_D(t)$ across the phase-cut dimmer is less than 0,1 x $V_M(t)$ during the entire conduction period.

Due to the low impedance of the phase-cut dimmer during the conducting period, the input voltage of the controlgear is almost equal to the mains voltage.

From the zero crossing of the mains to time t_{s1}, the controlgear provides a current path with a minimum current-carrying capability of I_{CG_STL}.

Table 12 – Nominal mains voltage from100 to 277 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Impedance
0 to t_{s1}	$Z_D = Z_{D\_min}$ $V_D(t) < \max(0{,}1 \times V_M(t), 10\ V)$

7.3.3.3 Electrical characteristics during the transition from the conducting to the non-conducting period

The transition from the conducting to the non-conducting state of the phase-cut dimmer starts at time t_{s1} and ends at time t_{s3}.

At the time t_{s1}, the impedance Z_D of the phase-cut dimmer should start to increase towards Z_{D_max}. From time t_{s1} to t_{s2}, the phase-cut dimmer should limit the current I_D to the value that is listed in Tables 13 to 17.

The minimum value for $t_t = t_{s2} - t_{s1}$ should be as listed in Tables 13 to 17.

Since the controlgear provides a current path with a minimum current-carrying capability of I_{CG_STL}, the voltage across the input terminals of the controlgear decreases towards zero and falls below the voltage V_{SW} at t_{s2} (see Figure 3).

NOTE 1 This requirement is to ensure that parasitic capacities of the installation, the active capacity C_f between the terminals of the phase-cut dimmer (see Figure 3) and a capacitor that might be assembled inside the controlgear and that is connected directly with the mains terminals of the controlgear are discharged in a reasonable time to allow the phase-cut dimmer to supply itself sufficiently.

NOTE 2 The ratio between the values for the period t_{s2} to t_{HW} as given in Tables 13 to 17 for the different mains voltages is proportional to the ratio of the relevant mains voltages. The values for I_{CG_STH} scale inversely with the mains voltage. The value for V_{SW} scales directly with the mains voltage. The value for I_{D_nc} is always 10% lower than the relevant I_{CG_STH}.

The slew rate SR should be calculated based on the measurement of the voltage slope of V_{CG} by measuring the time (dt) between V_{CG} = 0,8 x $V_{CG}(t_{s1})$ and $V_{CG} = V_{SW}$ and by calculating the differential voltage dV_{CG} = 0,8 x $V_{CG}(t_{s1}) - V_{SW}$.

When the voltage V_{CG} falls below V_{SW} (time t_{s2}), the controlgear provides a current path with a minimum current-carrying capability of I_{CG_STH}.

NOTE 3 The values for V_{SW} and I_{CG_STH} are selected to achieve a good compromise between the ability of the phase-cut dimmer to supply itself on one side and the appearing power loss in the controlgear on the other side.

NOTE 4 t_{s2} is defined by the time at which V_{CG} falls below V_{SW}. V_{CG} and I_D can be measured simultaneously with a 4-channel oscilloscope, and the value of I_D between t_{s1} and t_{s2} can be determined. The break in slope of V_D at t_{s2} (if such a break in slope exists) is not a criterion to define t_{s2}.

Table 13 – Nominal mains voltage 100 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Impedance
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \times V_M(t_{s1})$	$t = t_{s1}$: $Z_D = Z_{D\_min}$ $t_{s1} < t \leq t_{s2}$: Z_D increases towards Z_{D_max} $I_D \leq (I_{trans} \times P_{min}) / W$ with $dV_D/dt \leq$ 0,09 V/µs and I_{trans} = 2,8 mA
t_{s2} to t_{HW}	$P_{min} < 12$ W: $I_D(t) \leq I_{D\_nc} =$ $n \times 12{,}4$ mA/W x P_{min} $P_{min} \geq 12$ W: $I_D(t) \leq I_{D\_nc} = n \times 149$ mA

Table 14 – Nominal mains voltage 120 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Impedance
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \times V_M(t_{s1})$	$t = t_{s1}$: $Z_D = Z_{D\_min}$ $t_{s1} < t \leq t_{s2}$: Z_D increases towards Z_{D_max} $I_D \leq (I_{trans} \times P_{min}) / W$ with $dV_D/dt \leq$ 0,105 V/µs and I_{trans} = 2,3 mA
t_{s2} to t_{HW}	$P_{min} < 12$ W: $I_D(t) \leq I_{D\_nc} =$ $n \times$ 10,4 mA/W x P_{min} $P_{min} \geq 12$ W: $I_D(t) \leq I_{D\_nc} = n \times 124{,}2$ mA

Table 15 – Nominal mains voltage 200 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Impedance
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \cdot V_M(t_{s1})$	$t = t_{s1}$: $Z_D = Z_{D\_min}$ $t_{s1} < t \leq t_{s2}$: Z_D increases towards Z_{D_max} $I_D(t) \leq (I_{trans} \times P_{min}) / W$ with $dV_D/dt \leq$ 0,175 V/µs and I_{trans} = 1,4 mA
t_{s2} to t_{HW}	$P_{min} < 12$ W: $I_D(t) \leq I_{D\_nc} =$ $n \times 6{,}2$ mA/W x P_{min} $P_{min} \geq 12$ W: $I_D(t) \leq I_{D\_nc} = n \times 74{,}5$ mA

Table 16 – Nominal mains voltage 230 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Impedance
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \cdot V_M(t_{s1})$	$t = t_{s1}$: $Z_D = Z_{D\_min}$ $t_{s1} < t \leq t_{s2}$: Z_D increases towards Z_{D_max} $I_D(t) \leq (I_{trans}$ x $P_{min})$ / W with $dV_D/dt \leq$ 0,2 V/µs and I_{trans} = 1,2 mA
t_{s2} to t_{HW}	$P_{min} <$ 12 W: $I_D(t) \leq I_{D\_nc}$ = n x 5,4 mA/W x P_{min} $P_{min} \geq$ 12 W: $I_D(t) \leq I_{D\_nc} = n$ x 65 mA

Table 17 – Nominal mains voltage 277 V – Frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Phase-cut dimmer: Impedance
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \cdot V_M(t_{s1})$	$t = t_{s1}$: $Z_D = Z_{D\_min}$ $t_{s1} < t \leq t_{s2}$: Z_D increases towards Z_{D_max} $I_D(t) \leq (I_{trans}$ x $P_{min})$ / W with $dV_D/dt \leq$ 0,245 V/µs and I_{trans} = 1,0 mA
t_{s2} to t_{HW}	$P_{min} <$ 12 W: $I_D(t) \leq I_{D\_nc}$ = n x 4,5 mA/W x P_{min} $P_{min} \geq$ 12 W: $I_D(t) \leq I_{D\_nc} = n$ x 54 mA

7.3.3.4 Electrical characteristics during the non-conducting period

During the non-conducting period, the phase-cut dimmer should comply with the electrical characteristics listed in Tables 13 to 17.

The non-conducting period ends at the next zero crossing of the mains at time t_{HW}.

During this period, the controlgear provides a current path with a minimum current-carrying capability of I_{CG_STH}. At small input voltages of the controlgear when I_{CG_STH} cannot be reached due to the characteristics of its input circuitry (e.g. inrush current limiting elements), only its impedance Z_{CG} is defined.

During this period, the phase-cut dimmer should limit the current I_D to n x I_{D_nc} as listed in Tables 13 to 17, whereby I_{D_nc} is related to P_{min} of the phase-cut dimmer.

The controlgear may deactivate its current-carrying capability during the non-conducting period after it has not detected an input voltage waveform showing trailing edge characteristics for 100 ms.

NOTE This is for reducing power losses in case a controlgear is used without a phase-cut dimmer.

7.4 Electrical characteristics during the off state of a lighting system

The off state of a lighting system is when no lamp connected with a controlgear is emitting light.

To set a controlgear in the off state, the phase-cut dimmer should increase its impedance Z_D until the controlgear is not sufficiently supplied with power to operate the lamp.

A phase-cut dimmer that needs no supply during the off state of all connected controlgear may open the current loop of the system, for example by means of a mechanical switch.

A phase-cut dimmer that needs a power supply also during the off state of all connected controlgear requires that the connected controlgear provide a current path, although no lamp is operated (electronic off state), in order to provide power to the electronic circuits within the dimmer to enable returning to the on-state when demanded.

If none of the connected controlgear is able to provide the current carrying capability due to insufficient power, the impedance Z_{CG} of the controlgear will increase.

The phase-cut dimmer may reduce its impedance Z_D to supply power to the connected controlgear in order to reestablish a current carrying capability that carries the needed supply current I_{D_nc}.

By reducing Z_D, the voltage V_D will decrease and the voltage V_{CG} will increase, thus all connected controlgear is energized and the requested current path is generated in the system to carry the required supply current I_D of the phase-cut dimmer.

The controlgear provides a minimum current carrying capability of I_{PO} when the voltage V_{CG} is in the range of V_{PO} to V_{SW} (see Table 18). For voltages V_{CG} smaller than V_{PO} and higher than V_{SW}, the current carrying capability of the controlgear is not defined.

The controlgear does not operate the lamp when the voltage V_{CG} is below V_{SW}, so no light is emitted.

The phase-cut dimmer should limit the current to a level that ensures that the voltage V_{CG} that is applied to the controlgear does not exceed V_{SW}.

Table 18 – Currents and voltages for controlgear during the electronic off state

V_M [V]	100	120	200	230	277
V_{PO} [V]	15	15	30	30	30
I_{PO} [mA]	20	20	10	10	10
I_{PO_rms} [mA]	8	8	4	4	4

Values for voltages and currents are instantaneous values except I_{PO_rms}.

8 Test procedures

8.1 General

Devices supporting leading and trailing edge operation such as so called universal phase-cut dimmers should be tested for both operation modes.

To simplify the description of the test setups and the test procedures, testing conditions for dimmers related to specific moments in time are defined in degree phase angle related to the mains zero crossings. Thus, a definition of different values for the moments in time such as, for example, t_{s1}, t_{s2} or t_{HW} is not necessary for different mains frequencies.

To test the phase-cut dimmer, in some tests equivalent controlgear (EC_CG) should be used as indicated. This EC_CG should be constructed as shown in Annex A.

Table 19 – Parameters for testing purposes

V_M [V]	100	120	200	230	277
R_R	V_M^2 / P_{max}	V_M^2 / P_{max}	V_M^2 / P_{max}	V_M^2 / P_{max}	V_M^2 / P_{max}
V_{test} [V]	0 to 23	0 to 23	0 to 45	0 to 45	0 to 45
V_1 [V]	8	8	8	8	8
SR_L [V/µs]	Refers to Table 6				
α_L	90°				
β_L	120°				
SR_T [V/ms]	200	200	200	200	200
α_T	120°				

8.2 Tests for leading edge phase-cut dimmers

8.2.1 General

Tests concerning electrical characteristics should ensure compliance of devices with this document in terms of electrical behavior of phase-cut dimmers during different periods of the mains waveform according to 7.3.2.

8.2.2 Test related to the non-conducting phase

For this test, there are 2 different methods of testing the phase-cut dimmer current. Only one of these methods needs to be used when performing this test.

Method 1

A test circuit as shown in Figure 4 should be used to test the properties of the phase-cut dimmer during the non-conducting phase. The resistance of the resistor R_R should be chosen according to Table 19.

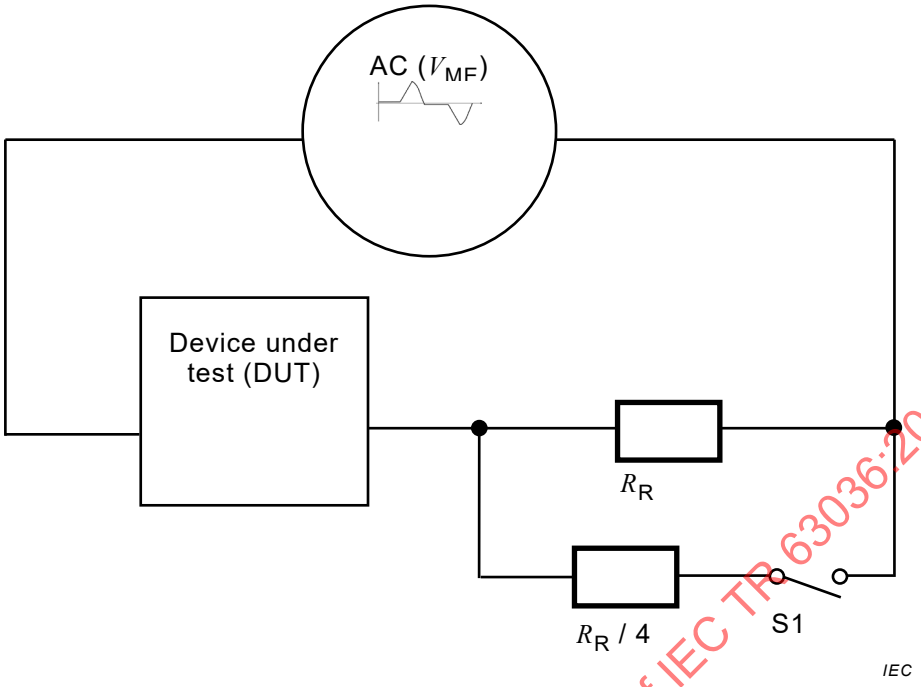

Figure 4 – Circuit to test the properties of the phase-cut dimmer during the non-conducting phase (Method 1)

Pre-condition: Control device applied to an AC test voltage source (V_{ME}) providing the relevant mains voltage according to Clause A.3 with the values of V_1, β_L and SR_T as given in Table 19. Switch S1 is open. Adjust the phase-cut dimmer so that the switch in the phase-cut dimmer is switched on at the time t_s (β1). Close switch S1. If necessary for the function of the phase-cut dimmer, apply for one minute the mains voltage V_M (e.g. for the calibration of universal phase-cut dimmer). Adjust the phase-cut dimmer close to the phase angle of t_s. S1 is opened in this phase. Change V_M to V_{ME} (according to Clause A.3) and close S1.
Time related to last zero crossing: 0 to t_s
Test: Measure I_D
Expected result: $I_D \leq I_{D\_nc}$ as listed in Tables 1 to 5 (I_{D_nc} depends on P_{min} and n given by the specification of the manufacturer)

To keep the test as simple as possible, the dimmer is connected to a test voltage which represents the voltage across the dimmer.

This test method covers the worst case scenario by using the worst controlgear, without having any parasitic effects caused by synthetic loads.

Therefore the voltage across the dimmer looks like a trailing edge waveform.

To reduce the influence on the current through the load taken by the dimmer, the impedance of the test voltage source should be as low as possible.

Due to the overcurrent protection of the dimmer, S1 is closed after the test voltage has been applied to the dimmer.

Method 2

Applicable test circuit, see Figure 5.

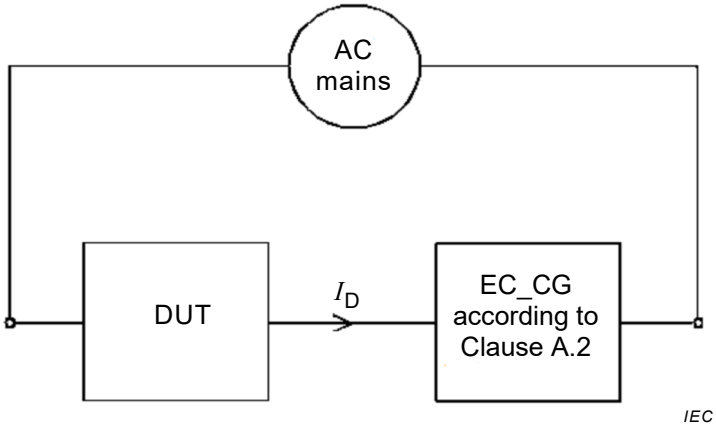

Figure 5 – Circuit to test the properties of the phase-cut dimmer during the non-conducting phase (Method 2)

Pre-condition: Phase-cut dimmer loaded with the circuit of Figure B.1, system powered with relevant mains voltage. Values of R20 and C20 should be set according to Annex B using the values of I_{D_nc} given in Tables 1 to 5.
Time related to last zero crossing: 0 to t_s
Test: Measure I_D
Expected result: $I_D \leq I_{D\_nc}$ as listed in Tables 1 to 5 (I_{D_nc} depends on the P_{min} and n given by the specification of the manufacturer)

8.2.3 Test related to the transition from the non-conducting to the conducting phase

A test circuit as shown in Figure 6 should be used to test the phase-cut dimmer's properties during the transition from the non-conducting to the conducting phase.

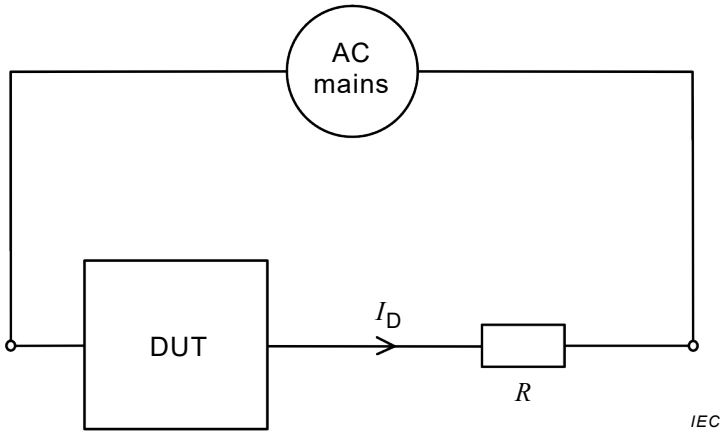

Figure 6 – Circuit to test the properties of the phase-cut dimmer during the transition from the non-conducting to the conducting phase

Pre-condition: Phase-cut dimmer loaded with a resistive load R having a maximum resistance R_R (see Table 19) as shown in Figure 6, system powered with relevant mains voltage, phase-cut dimmer adjusted to the conduction angle of 90°.
Time related to last zero crossing: t_s
Test: Measure V_D or voltage across resistor R over time
Expected result: Absolute value of voltage slope across the DUT (V_D) or R does not exceed the limits given in Table 6.

8.2.4 Test related to the conducting phase

A test circuit as shown in Figure 6 should be used to test the phase-cut dimmer's properties during the conducting phase.

Pre-condition: A phase-cut dimmer loaded with a resistive load R having a maximum resistance R_R (see Table 19) as shown in Figure 6, system powered with relevant mains voltage, phase-cut dimmer adjusted to the conduction angle of 120°. This test should be performed for the minimum and maximum load, such as R_{Rmax} (V_M^2/P_{max}) and R_{Rmin} (V_M^2/P_{min})
Time related to last zero crossing: t_s to t_{HW}
Test: Measure V_D over time
Expected result for $V_M(t) > 11V$: $V_D(t) < \max(0{,}1 \times V_M(t), 10V)$

8.3 Tests for trailing edge phase-cut dimmers

8.3.1 General

Tests concerning the electrical characteristics should ensure compliance of devices with this document in terms of electrical behavior of phase-cut dimmers during different periods of the mains waveform according to 7.3.3.

8.3.2 Test related to the conducting phase

Applicable test circuit, see Figure 6.

Pre-condition: Phase-cut dimmer loaded with a resistive load having a maximum resistance R_R (see Table 7), system powered with relevant mains voltage, phase-cut dimmer adjusted to the conduction angle of 120°. This test should be performed for the minimum and maximum load, such as R_{Rmax} (V_M^2/P_{max}) and R_{Rmin} (V_M^2/P_{min})
Time related to last zero crossing: 0 to t_{s1}
Test: Measure V_D over time
Expected result for $V_M(t) > 11V$: $V_D(t) < \max(0,1 \times V_M(t), 10V)$

8.3.3 Test related to the transition from the conducting phase to the non-conducting phase and related to the non-conducting phase

For this test, there are 2 different methods of testing the phase-cut dimmer current. Only one of these methods needs to be used when performing this test.

Method 1:

A test circuit as shown in Figure 4 should be used to test the phase-cut dimmer's properties during the transition from the conducting phase to the non-conducting phase and the non-conducting phase.

Pre-condition: A control device applied to an AC test voltage source (V_{ME}) providing the relevant mains voltage according to Clause A.2 with the values of V_1, α_T and SR_T as given in Table 19. S1 is open. Adjust the phase-cut dimmer so that the switch-off takes place at time t_{S1}. Close S1. If necessary for the function of the phase-cut dimmer, expand (V_{ME}) so that after power up for a period of 1 min, the nominal mains voltage is applied (e.g. for the calibration of universal phase-cut dimmers). Adjust the phase-cut dimmer close to the phase angle of t_1. S1 is opened in this phase. Close S1 when the AC test voltage source (V_{ME}) according to Annex A is applied.
Time related to last zero crossing: t_{s1} to t_{s2} and t_{S2} to t_{HW}
Test: Measure I_D from t_{s1} to t_{HW}
Expected results: From t_{s1} to t_{s2}: $I_D \leq (I_{trans} \times P_{min})$ / W as listed in Tables 13 to 17 From t_{s2} to t_{HW}: $I_D \leq I_{D\_nc}$ as listed in Tables 13 to 17 (I_{D_nc} depends on P_{min} and n given by the specification of the manufacturer)

Method 2:

Applicable test circuit, see Figure 5.

Pre-condition: Phase-cut dimmer loaded with the circuit of Figure B.1, system powered with relevant mains voltage. Values of R20 and C20 should be set according to Annex B, using the values of I_{D_nc} and SR given in Tables 13 to 17.
Time related to last zero crossing: t_{s1} to t_{s2} and t_{S2} to t_{HW}
Test: Measure I_D from t_{s1} to t_{HW}
Expected results: From t_{s1} to t_{s2}: $I_D \leq (I_{trans}$ x $P_{min})$ / W as listed in Tables 13 to 17 From t_{s2} to t_{HW}: $I_D \leq I_{D\_nc}$ as listed in Tables 13 to 17 (I_{D_nc} depends on P_{min} and n given by the specification of the manufacturer)

8.4 Tests for characteristics during electronic off state

Tests concerning the electrical characteristics should ensure compliance of devices with this document in terms of electrical behavior of phase-cut dimmers during the electronic off-state of a lighting system according to 7.3.

Applicable test circuit, see Figure 7.

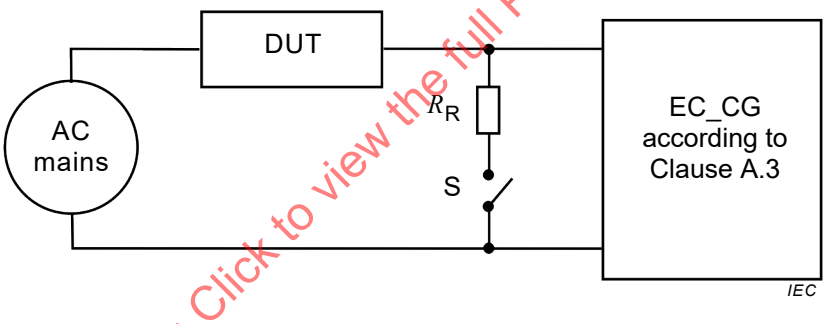

Figure 7 – Circuit to test the properties of the phase-cut dimmer during the electronic off-state

Pre-condition: Phase-cut dimmer connected to an AC source (V_M). Configure the phase-cut dimmer to be in the electronic off state before connecting it to the circuit shown in Figure 7. For example, the switch S and the resistance R_R as shown in Figure 7 can be used. After this initial phase, set the phase-cut dimmer to the electronic off state and open switch S.
Test: Measure V_{CG} and I_{PO_rms}
Expected results: $V_{CG} < V_{SW}$ as listed in Tables 1 to 5, 7 to 11, 13 to 17 $I_{D\_RMS} \leq I_{PO\_rms}$ as listed in Table 18